### Course Structure and Syllabus

#### I Semester

<table>
<thead>
<tr>
<th>Category</th>
<th>Course Title</th>
<th>Int. marks</th>
<th>Ext. marks</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>PC-1</td>
<td>Advanced Digital System Design</td>
<td>25</td>
<td>75</td>
<td>4</td>
<td>0</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>PC-2</td>
<td>Coding Theory and Techniques</td>
<td>25</td>
<td>75</td>
<td>4</td>
<td>0</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>PC-3</td>
<td>Broadband Communications</td>
<td>25</td>
<td>75</td>
<td>4</td>
<td>0</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>PE-1</td>
<td>Real Time Operating Systems</td>
<td>25</td>
<td>75</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>Image and Video Processing</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Spread Spectrum Communications</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PE-2</td>
<td>Advanced Computer Architecture</td>
<td>25</td>
<td>75</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>Advanced Digital Signal Processing</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Optical Communications and Networks</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OE-1</td>
<td>*Open Elective – I</td>
<td>25</td>
<td>75</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>Laboratory I</td>
<td>Digital System Design Lab</td>
<td>25</td>
<td>75</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>Seminar I</td>
<td>Seminar</td>
<td>100</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td>2</td>
</tr>
</tbody>
</table>

**Total** 275 525 21 0 6 25

#### II Semester

<table>
<thead>
<tr>
<th>Category</th>
<th>Course Title</th>
<th>Int. marks</th>
<th>Ext. marks</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>PC-4</td>
<td>Design of Fault Tolerant Systems</td>
<td>25</td>
<td>75</td>
<td>4</td>
<td>0</td>
<td>1</td>
<td>4</td>
</tr>
<tr>
<td>PC-5</td>
<td>Detection and Estimation Theory</td>
<td>25</td>
<td>75</td>
<td>4</td>
<td>0</td>
<td>1</td>
<td>4</td>
</tr>
<tr>
<td>PC-6</td>
<td>Wireless Communications and Networks</td>
<td>25</td>
<td>75</td>
<td>4</td>
<td>0</td>
<td>1</td>
<td>4</td>
</tr>
<tr>
<td>PE-3</td>
<td>System on Chip Architecture</td>
<td>25</td>
<td>75</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>Software Defined Radio</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Cellular and Mobile Communications</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PE4</td>
<td>Network Security And Cryptography</td>
<td>25</td>
<td>75</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>Digital Signal Processors and Architectures</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>EMI / EMC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>OE-2</td>
<td>*Open Elective – II</td>
<td>25</td>
<td>75</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>Laboratory II</td>
<td>Wireless Communications and Networks Lab</td>
<td>25</td>
<td>75</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>Seminar II</td>
<td>Seminar</td>
<td>100</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td>2</td>
</tr>
</tbody>
</table>

**Total** 275 525 21 0 6 25
### III Semester

<table>
<thead>
<tr>
<th>Course Title</th>
<th>Int. marks</th>
<th>Ext. marks</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technical Paper Writing</td>
<td>100</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>Comprehensive Viva-Voce</td>
<td>0</td>
<td>100</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>Project work Review I</td>
<td>100</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>22</td>
<td>8</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>200</strong></td>
<td><strong>100</strong></td>
<td>0</td>
<td>3</td>
<td>22</td>
<td>14</td>
</tr>
</tbody>
</table>

### IV Semester

<table>
<thead>
<tr>
<th>Course Title</th>
<th>Int. marks</th>
<th>Ext. marks</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Project work Review II</td>
<td>100</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>24</td>
<td>8</td>
</tr>
<tr>
<td>Project Evaluation (Viva-Voce)</td>
<td>0</td>
<td>200</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>16</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>100</strong></td>
<td><strong>200</strong></td>
<td>0</td>
<td>0</td>
<td>24</td>
<td>24</td>
</tr>
</tbody>
</table>

*Open Elective subjects must be chosen from the list of open electives offered by various departments.*
UNIT - I
Processor Arithmetic: Two's Complement Number System - Arithmetic Operations; Fixed point Number System; Floating Point Number system - IEEE 754 format, Basic binary codes.

UNIT - II

UNIT - III
Sequential Logic - Latches and Flip-Flops, Sequential logic circuits - timing analysis (Set up and hold times), State machines - Mealy & Moore machines, Analysis, FSM design using D Flip-Flops, FSM optimization and partitioning; Synchronizers and metastability. FSM Design examples: Vending machine, Traffic light controller, Washing machine.

UNIT - IV
Subsystem Design using Functional Blocks (1) - Design (including Timing Analysis) of different logical blocks of varying complexities involving mostly combinational circuits:
- ALU
- 4-bit combinational multiplier
- Barrel shifter
- Simple fixed point to floating point encoder
- Dual Priority encoder
- Cascading comparators

UNIT - V
Subsystem Design using Functional Blocks (2) - Design, (including Timing Analysis) of different logical blocks of different complexities involving mostly sequential circuits:
- Pattern (sequence) detector
- Programmable Up-down counter
- Round robin arbiter with 3 requesters
- Process Controller
- FIFO

TEXT BOOKS:

*Note1: VHDL and ABEL are not part of this course.
*Note2: SSI & MSI ICs listed in data books are not part of this course.
UNIT – I
Coding for Reliable Digital Transmission and storage: Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, Types of Errors, Error Control Strategies.

Linear Block Codes: Introduction to Linear Block Codes, Syndrome and Error Detection, Minimum Distance of a Block code, Error-Detecting and Error-correcting Capabilities of a Block code, Standard array and Syndrome Decoding, Probability of an undetected error for Linear Codes over a BSC, Hamming Codes. Applications of Block codes for Error control in data storage system

UNIT - II
Cyclic Codes : Description, Generator and Parity-check Matrices, Encoding, Syndrome Computation and Error Detection, Decoding ,Cyclic Hamming Codes, Shortened cyclic codes, Error-trapping decoding for cyclic codes, Majority logic decoding for cyclic codes.

UNIT – III
Convolutional Codes: Encoding of Convolutional Codes, Structural and Distance Properties, maximum likelihood decoding, Sequential decoding, Majority- logic decoding of Convolution codes. Application of Viterbi Decoding and Sequential Decoding, Applications of Convolutional codes in ARQ system.

UNIT – IV
Turbo Codes: LDPC Codes- Codes based on sparse graphs, Decoding for binary erasure channel, Log-likelihood algebra, Brief propagation, Product codes, Iterative decoding of product codes, Concatenated convolutional codes- Parallel concatenation, The UMTS Turbo code, Serial concatenation, Parallel concatenation, Turbo decoding

UNIT - V
Space-Time Codes: Introduction, Digital modulation schemes, Diversity, Orthogonal space- Time Block codes, Alamouti’s schemes, Extension to more than Two Transmit Antennas, Simulation Results, Spatial Multiplexing : General Concept, Iterative APP Preprocessing and Per-layer Decoding, Linear Multilayer Detection, Original BLAST Detection, QL Decomposition and Interface Cancellation, Performance of Multi – Layer Detection Schemes, Unified Description by Linear Dispersion Codes.

TEXT BOOKS:

REFERENCE BOOKS:
1. Bernard Sklar, “Digital Communications-Fundamental and Application”, PE.
3. Salvatore Gravano, “Introduction to Error Control Codes”, Oxford
UNIT – I

UNIT – II

UNIT – III
ATM: Overview, Virtual channels, Virtual paths, VP and VC switching, ATM cells, Header format, Generic flow control, Header error control, Transmission of ATM cells, Adaptation layer, AAL services and protocols.

UNIT – IV
ATM switching: ATM switching building blocks, ATM cell processing in a switch, Matrix type switch, Input, Output buffering, Central buffering, Performance aspects of buffering switching networks.

UNIT – V
ATM Traffic and congestion Control: Requirements for ATM Traffic and Congestion Control, Cell-Delay Variation, ATM Service Categories, Traffic and Congestion Control Framework, Traffic Control, Congestion Control

Text Book:
UNIT – I
Introduction: Introduction to UNIX/LINUX, Overview of Commands, File I/O, (open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT – II

UNIT – III
Objects, Services and I/O: Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem

UNIT – IV

UNIT – V
Case Studies of RTOS: RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, and Tiny OS, and Android OS.

TEXT BOOKS:

REFERENCE BOOKS
UNIT –I
Fundamentals of Image Processing and Image Transforms: Basic steps of Image Processing System Sampling and Quantization of an image, Basic relationship between pixels.
Image Segmentation: Segmentation concepts, Point, Line and Edge Detection, Thresholding, Region based segmentation.

UNIT –II
Frequency domain methods: Basics of filtering in frequency domain, Image smoothing, Image sharpening, Selective filtering.

UNIT –III
Image Compression: Image compression fundamentals - Coding Redundancy, Spatial and Temporal redundancy, Compression models: Lossy & Lossless, Huffman coding, Bit plane coding, Transform coding, Predictive coding, Wavelet coding, Lossy Predictive coding, JPEG Standards.

UNIT -IV

UNIT –V
2-D Motion Estimation: Optical flow, General Methodologies, Pixel Based Motion Estimation, Block-Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

TEXT BOOKS:

REFERENCE BOOKS:
UNIT -I

Binary Shift Register Sequences for Spread Spectrum Systems: Introduction, Definitions, Mathematical Background and Sequence Generator Fundamentals, Maximal Length Sequences, Gold Codes.

UNIT -II

UNIT -III
Initial Synchronization of the Receiver Spreading Code: Introduction, Problem Definition and the Optimum Synchronizer, Serial Search Synchronization Techniques, Synchronization using a Matched Filter, Synchronization by Estimated the Received Spreading Code.

UNIT -IV


UNIT -V


TEXT BOOKS:

REFERENCE BOOKS:
UNIT -I
Instruction set principles and examples- Introduction, Classifying instruction set- Memory addressing-type and size of operands, Operations in the instruction set.

UNIT –II
Pipelines: Introduction, Basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

UNIT -III
Instruction Level Parallelism the Hardware Approach: Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo’s approach, Branch prediction, high performance instruction delivery- hardware based speculation.
ILP Software Approach: Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT –IV
Multi Processors and Thread Level Parallelism: Multi Processors and Thread level Parallelism-Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT –V
Inter Connection and Networks: Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.
Intel Architecture: Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

TEXT BOOKS:

REFERENCE BOOKS:
UNIT –I
Review of DFT, FFT, IIR Filters and FIR Filters: Multi Rate Signal Processing: Introduction, Decimation by a factor D, Interpolation by a factor I, Sampling rate conversion by a rational factor I/D, Multistage Implementation of Sampling Rate Conversion, Filter design & Implementation for sampling rate conversion.

UNIT –II

UNIT -III
Non-Parametric Methods of Power Spectral Estimation: Estimation of spectra from finite duration observation of signals, Non-parametric Methods: Bartlett, Welch & Blackman-Tukey methods, Comparison of all Non-Parametric methods

UNIT –IV
Implementation of Digital Filters: Introduction to filter structures (IIR & FIR), Frequency sampling structures of FIR, Lattice structures, Forward prediction error, Backward prediction error, Reflection coefficients for lattice realization, Implementation of lattice structures for IIR filters, Advantages of lattice structures.

UNIT –V

TEXT BOOKS:

REFERENCE BOOKS:
2. P.P. Vaidyanathan “Multi Rate Systems and Filter Banks”, Pearson Education.
UNIT I
Optical Fibers: Structures, waveguiding and Fabrication: Nature of Light, Basic optical laws and definitions, Single mode fibers, Graded index fiber structure, Attenuation, Signal Dispersion in fibers.
Optical Sources- LEDs, Laser Diodes, Line Coding.

UNIT II
Photo detectors: Photo detector Noise, Detector Response Time, Avalanche Multiplication Noise.
WDM Concepts and Components: Passive optical Couplers, Isolators and Circulators

UNIT III
Digital Links: Point to point links, power penalties, error control, Coherent detection, Differential Quadrature Phase Shift Keying.
Analog Links: Carrier to noise ration, Multichannel Transmission Techniques, RF over Fiber, Radio over fiber links, Microwave Photonics.

UNIT IV

UNIT V
Performance Measurement and Monitoring: Measurement standards, Basic Test Equipment, Optical power measurement, Optical fiber characterization, Eye diagram tests, optical time domain reflectometer, optical performance monitoring, optical fiber system performance measurements.

TEXTBOOKS:

REFERENCE BOOKS:
Part –I
Programming can be done using any compiler. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front end tools.

1. HDL code to realize all the logic gates
2. Design and Simulation of adder, Serial Binary Adder, Multi Precision Adder, Carry
3. Look Ahead Adder.
4. Design of 2-to-4 decoder
5. Design of 8-to-3 encoder (without and with parity)
6. Design of 8-to-1 multiplexer
7. Design of 4 bit binary to gray converter
8. Design of Multiplexer/ Demultiplexer, comparator
9. Design of Full adder using 3 modeling styles
10. Design of flip flops: SR, D, JK, T
11. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequence counter
13. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
14. Design of 4-Bit Multiplier, Divider.
15. Design of ALU to Perform – ADD, SUB, AND-OR, 1’s and 2’s Compliment,
16. Multiplication, and Division.
17. Design of Finite State Machine.
18. Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits.

Part –II
1. Static and Dynamic Characteristics of CMOS Inverter
2. Implementation of EX-OR gate using complementary CMOS, Psedo-NMOS, Dynamic and domino logic style
3. Implementation of Full Adder using Transmission Gates